A DIGITAL CORRELATOR

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A DIGITAL CORRELATOR

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ABSTRACT: The operation and circuitry of a correlator, which forms a portion of a lock-in system, is discussed in detail. Clipper amplifiers convert analog input signals to digital signals, polarity coincidence detectors act as multipliers, and binary counters serve as integrators to give a digital output representing a single point on a correlogram.

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This report describes the operation and circuitry of a solid-state digital correlator. The work on this project was funded under Task No. NOL 396, Job Order No. 942-0896. This report will be of interest to those who are doing work in data processing and servo systems.

R. E. ODENING
Captain, USN
Commander

Z. I. SLAWSKY
By direction

CONTENTS

ILLUSTRATIONS

INTRODUCTION

1. This report discusses the operation of a digital correlator which forms a portion of a lock-in or servo system described in reference (a). Input signals in analog form are converted to digital signals in binary form by means of clipper amplifiers. The information content of the signals is then represented only by the axis-crossings as a function of time. The elimination of the amplitude information can be shown to have only a minor effect on the correlation function for the small signal-to-noise ratios used provided the input signal is sampled at the Shannon rate or higher, reference (b). A polarity coincidence detector, acting as a multiplier, in conjunction with a 1 Mc clock signal gives a sampled output of the coincidence of the input signals. The sampled output in the form of negative rectangular pulses 0.5 μsec wide is fed into a binary counter which acts as an integrator by dividing down the pulse frequency to a lower rate. Thus the value of one point on the correlogram will be indicated in digital form at the output of the counter in terms of the number of pulses per second. This output signal is then fed to the remainder of the servo system where its utilization is described in references (a), (c), (d) and (e). In other applications the output of this correlator could be converted from digital to analog form by the simple employment of an RC-integrator in place of the binary counter. In its application here, it is left in digital form to be compatible with the remainder of the lock-in system. The advantage of digital systems over analog systems is the greater accuracy obtainable for a given circuit complexity. In addition since information is contained simply in the presence or absence of pulses, no stringent requirements are placed on the dc power supplies operating the circuitry.

OPERATION

2. The block diagram in Figure 1 shows two complete correlators as employed in the Digital Lock-in System. Inputs 1 and 2 form the input of one correlator while Inputs 2 and 3 form the input of the second. A complete single correlator is composed of two clipper amplifiers, a polarity coincidence detector, a binary counter, and the 1.0 Mc clock oscillator. In this system Input No. 2 and the clock oscillator are common to both correlators. Since both correlators operate identically, the discussion will be confined to the one system operating from Inputs Nos. 1 and 2.

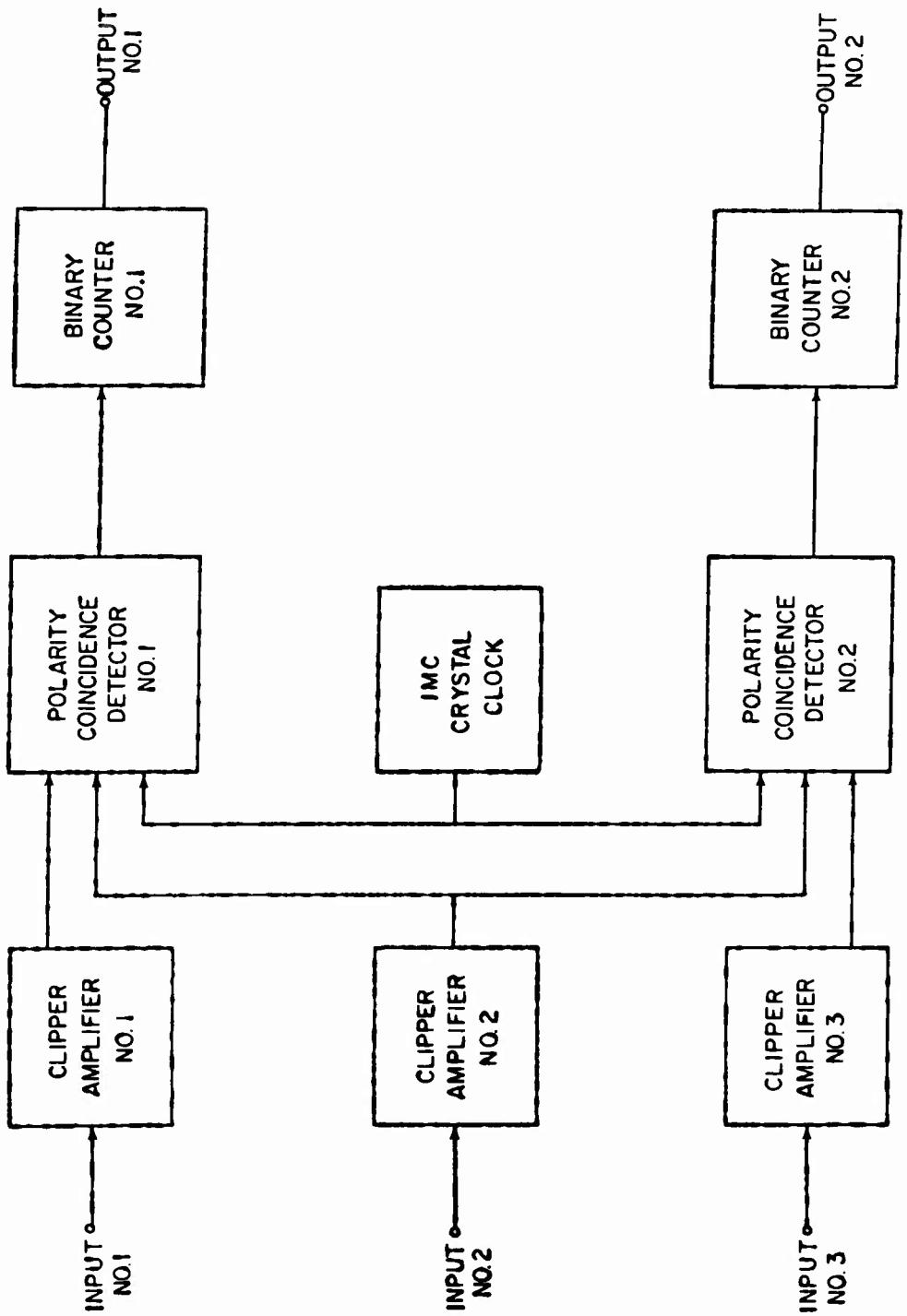

FIG. 1 BLOCK DIAGRAM OF TWO DIGITAL CORRELATORS.

3. The two analog signals in this application have an octave band-width of 2.5 to 5.0 kc and are fed into Inputs 1 and 2 where they are severely clipped by the clipper amplifiers. This is accomplished by four stages of amplification in which each stage is designed to amplify as well as symmetrically clip small positive and negative excursions. This cascaded action produces clean rectangular pulses with sharp rise and fall times at the amplifier output. The axis-crossings of the digitalized output can be made to correspond with the analog axis-crossings to within 0.1 μsec by proper adjustment of the symmetry controls on each stage of the amplifier. The outputs of Clipper Amplifiers No. 1 and 2 are directed to Polarity Coincidence Detector No. 1 where the two signals are compared along with the 1.0 Mc pulses which are generated by the crystal clock. If the polarity of the two clipped signals are identical, either both negative or both positive, the coincidence detector will allow the clock pulses to be passed to Binary Counter No. 1. If the clipped signals are opposite in polarity, the clock pulses will be prohibited from passing to the counter. This action causes the coincidence detector to produce a sampled output of the coincidence waveform resulting from the true binary product of the two clipped signals. As an example if the two input analog signals are incoherent, the two clipped signals will tend to be in agreement 50% of the time. Thus the output of the coincidence detector will produce an average of 500,000 pulses per second, and they will occur at random intervals if the input signals are essentially noise. Thus an average rate of 500,000 pulses per second corresponds to 0% correlation. If the input signals are perfectly coherent, the output pulse rate would then be exactly 1 megacycle per second, corresponding to 100% correlation. Similarly a zero output pulse rate would represent a 100% negative correlation. More often, of course, the average pulse rate will lie somewhere in between these extreme values depending on the degree of correlation of the input signals.

4. In the application, for which this system was designed, a coherent detection type of cross-correlation technique was used. A signal mixed with noise was fed to Input No. 2 while a noise-free delayed replica of that signal was fed to Input No. 1. The average number of pulses per second generated by the coincidence detector then depends upon the signal-to-noise ratio of Input No. 2 and the time delay relationship between the two coherent signals in each channel. The amount by which the average pulse rate differs from the uncorrelated value of 500,000 is the effective quantity in the operation of the servo system. The 500,000 average pulse

rate due to the presence of the noise is useless to the system but is undistinguishable from the valid pulses on a short time basis. It is therefore necessary to use some form of integration to average out the noise pulses and obtain an indication of the remaining signal pulses which are the ones containing the information necessary to operate the lock-in system.

5. The integration in this correlator is accomplished by the binary counter which follows the coincidence detector output. The integration time is proportional to 2^n, where n is the number of stages of the counter. Since the input pulse rate is about 500,000 pps, the effective integration time may be considered to be approximately 2×2^n μsec, which is also the average period of the output pulses. In the subject correlator, the counter has a maximum number of 17 stages. Output taps on each stage provide a means for varying the integration time as desired up to the maximum given by 17 stages. The function of the counter as an integrator is to count a large sample space and then give a lower pulse rate at its output to indicate the trend of the decisions appearing at its input. Whereas a single pulse out of the coincidence detector may be either a right or wrong decision, the single output pulse from the counter represents the majority opinion of a large number of pulses or decisions, 131,072 in the case of 17 stages. Thus each counter output pulse would tend to be a correct decision.

6. Two of these correlators as shown in Figure 1 are needed to operate the Digital Lock-in System. The signals for Inputs No. 1 and 3 are identical pseudo-random signals with an infinite signal-to-noise ratio. One of these signals is delayed a nominal amount τ with respect to the signal portion of Input No. 2, while the other signal is advanced the same nominal amount τ relative to Input No. 2. The values of the correlation function generated by the two coincidence detectors will be identical: (1) if the correlation function is symmetrical about zero delay, and (2) if the advance and delay times are the same. The derivatives of the correlation function at these identical delays have opposite signs so that when the two τ's are not quite equal, there will be a difference in the average pulse rate from the two coincidence detectors. It is this difference in rate which causes the servo system to make corrections. The pulses from Output No. 1 by means of additional circuitry described in reference (c) cause a servo oscillator, reference (f), to increase its frequency, while the pulses from Output No. 2 cause the oscillator to decrease its frequency. If the pulse rate from each output is the same, the oscillator does not change its frequency. But if either of the outputs has a higher rate

than the other, the oscillator will gradually increase or decrease its frequency as commanded until the pulse rate of each output is once again the same. The oscillator will then stay at the new frequency until the output rates from the two counters differ. The combined action of the two complete correlators effectively averages out or eliminates the pulses resulting from incoherency in the input signal while utilizing the pulses expressing coherency.

CIRCUIT DETAILS

7. A detailed discussion of the various circuits employed in the correlators will now be given. Three identical clipper amplifiers are employed. The circuit diagram of one of these is shown in Figure 2. Four emitter-coupled amplifier stages in cascade were chosen to perform the clipping action on the input analog signals. These stages are made up of the pairs of transistors Q_2-Q_3, Q_4-Q_5, Q_6-Q_7, and Q_8-Q_9. This type amplifier produces a clean rectangular and symmetrical clipping action. It also has no tendency toward overload distortion with large input signals until the peak-to-peak amplitude exceeds the available "B" supply. An emitter follower Q_1 at the input provides a relatively high input impedance, while another emitter follower Q_{10} is used at the output to give a low output impedance. A sinusoidal signal of a few millivolts rms at the input will begin to show a clipped signal at the output. A 10 mv signal will produce a good square wave at the output. To prevent extremely large signals from reaching the first emitter-coupled stage, a diode clipper is employed ahead of the emitter follower. Since these are silicon diodes, they start conducting when their forward potential reaches approximately 0.5 volt. Connected back-to-back as shown, they prevent any signal larger than 1 volt peak-to-peak from appearing at the input of the first stage. The clipped output signal of the amplifier will have a constant peak-to-peak value of about 3 volts for a six volt B-supply and for any input signal from 5 mv to 50 volts rms. The equivalent input noise of this amplifier is approximately 300 μv rms. The rise and fall times of the output signal are less than 0.1 μs each for a 0.3 volt rms sinusoidal input signal. Adjustable trim potentiometers are provided on each emitter-coupled amplifier stage to adjust the symmetry of the output waveform. These controls should be adjusted in order starting at the last stage. An oscilloscope is attached to the collector stage of the output and the waveform observed at that point. A sinusoidal signal just large enough to start to produce clipping is then introduced at the input of the amplifier. The potentiometer of

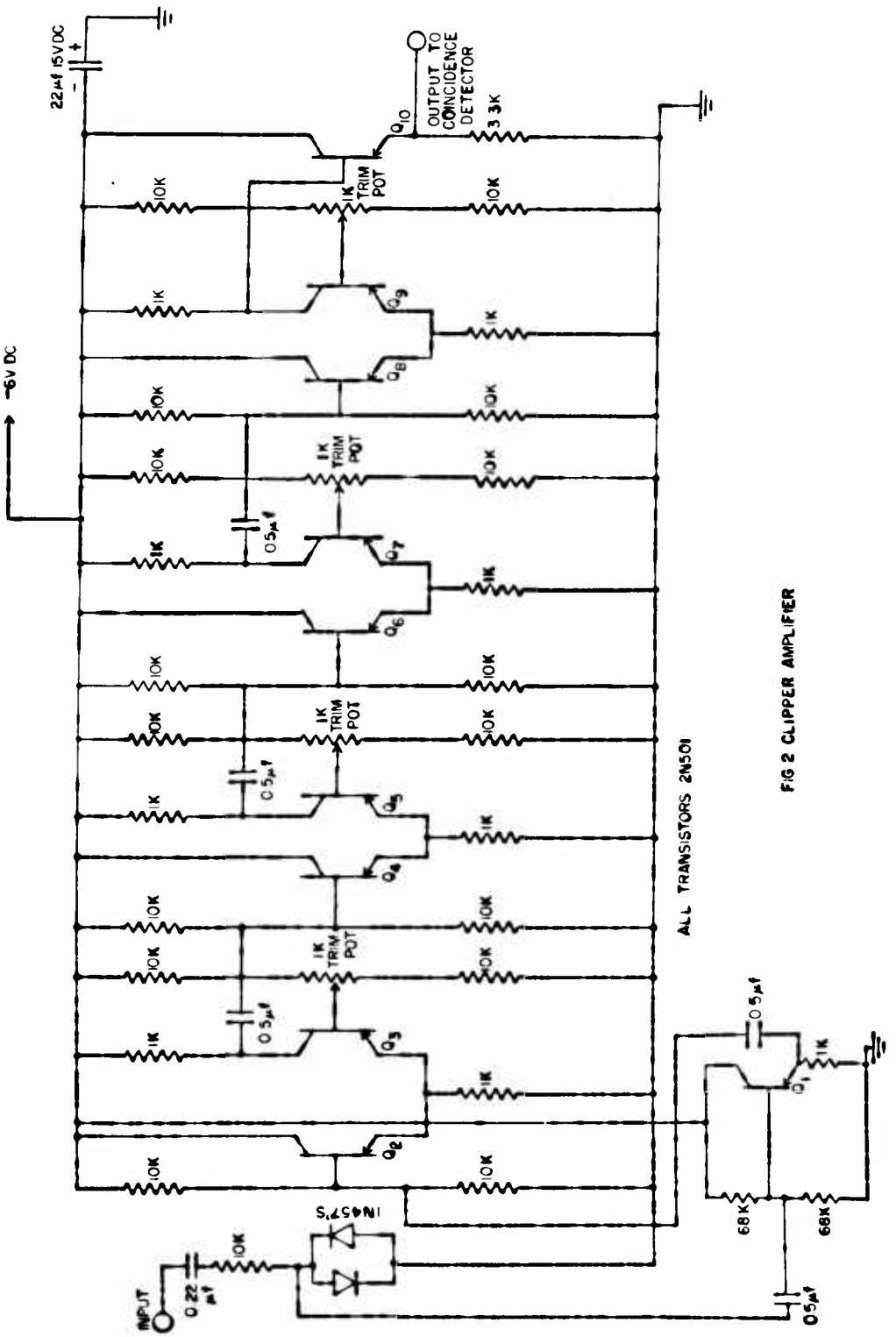

FIG 2 CLIPPER AMPLIFIER

the last stage is adjusted to produce symmetrical clipping of the signal. The oscilloscope should then be moved back to the next stage and the above procedure repeated until all four stages have been aligned. This adjustment should suffice until one of the transistors has to be replaced. It is possible to adjust the axis-crossings of the output waveforms of the three clipper amplifiers to within approximately 0.1 μsec when a common signal is fed to the inputs of the three amplifiers.

8. The circuit diagram of Figure 3 shows the 1 Mc crystal clock oscillator and the two polarity coincidence detectors. The oscillator is a type of multivibrator circuit formed by transistors Q_{11} and Q_{12}. A 1 Mc quartz crystal is used as the feedback element to provide a high degree of frequency stability to the circuit. A flip-flop shaper composed of transistors Q_{13} and Q_{14} serves to square the oscillator output as well as act as a buffer stage for the oscillator. Three more identical shapers composed of transistors Q_{15} through Q_{20} act to improve the output waveforms of the three clipper amplifiers after transmission between circuit boards. In addition these four shapers serve to supply uniform signals to the two polarity coincidence detectors. The rise and fall times of the rectangular signals from the shapers are extremely rapid being on the order of 30 nanoseconds. Each polarity coincidence detector or diode detector contains two "and" circuits of three diodes each. Each "and" circuit provides a negative output pulse when its three inputs are negative. The two "and" circuits are supplied from opposite phases of the input signal shaper flip-flops so that one produces a negative output when positive signal coincidence occurs and the other gives a similar negative output for negative coincidence. The output of the two "and" circuits are added together in an "or" circuit to produce a negative pulse whenever either "and" circuit indicates input signal polarity agreement. The "or" circuits are each composed of two emitter followers and two diodes connected to their outputs. Transistors Q_{21} and Q_{22} are associated with one of the "or" circuits and Q_{24} and Q_{25}, with the other. The polarity coincidence detector used here is essentially a sampling circuit since its output supplies a series of 1 Mc clock oscillator pulses when the inputs are in agreement and no output pulses when the inputs are in disagreement. Two emitter followers Q_{23} and Q_{26} provide a low output impedance for each of the polarity coincidence detectors. These outputs drive the two binary counters which act as integrators.

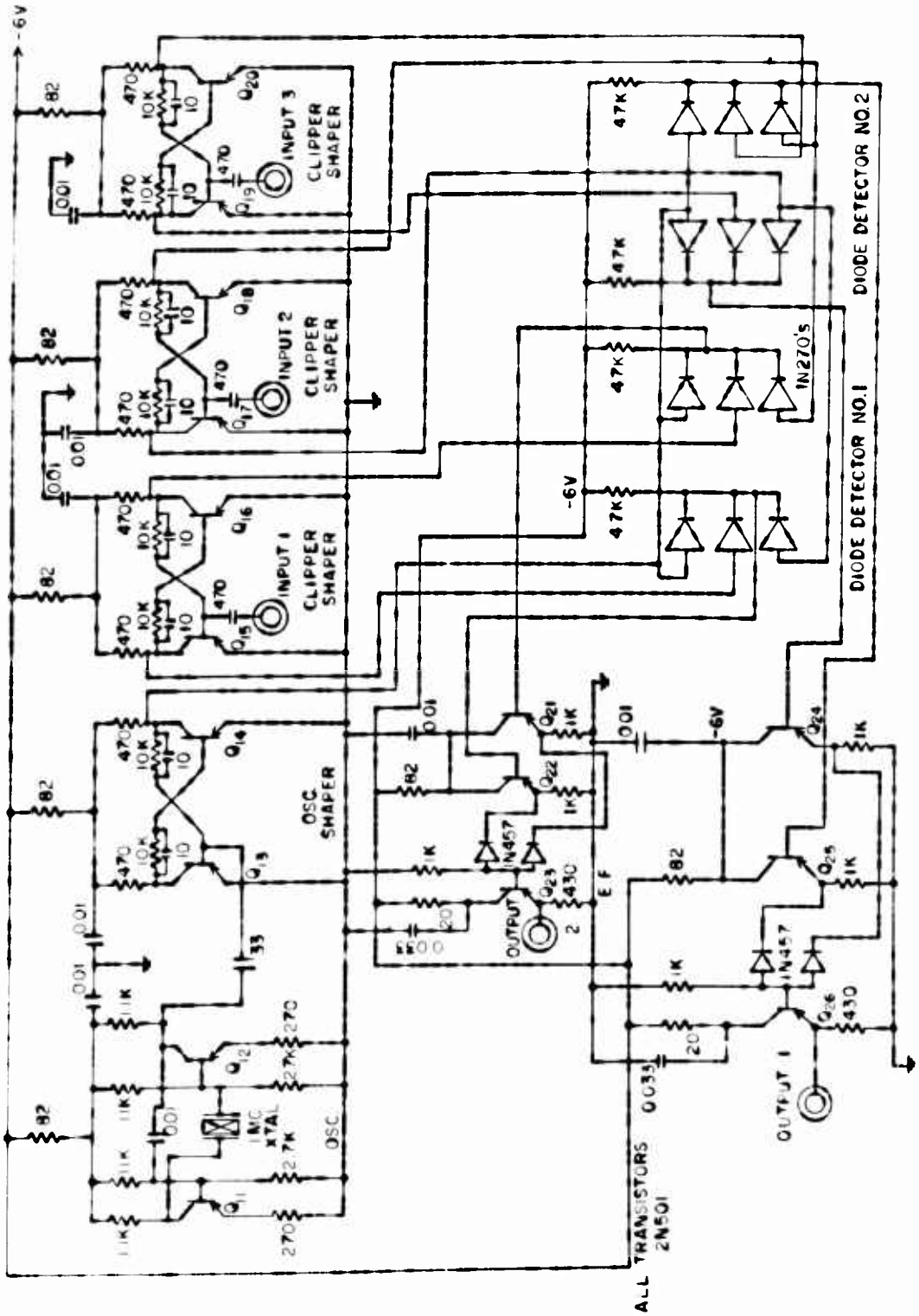

FIG. 3 I MC. OSC. & COINCIDENCE DETECTORS NO.1 AND NO.2

9. An abridged circuit diagram of one of the binary counters is shown in Figure 4. The output signals from the polarity coincidence detectors generally consist of complete 0.5 μsec negative pulses from the 1 Mc clock oscillator randomly grouped or spaced. Occasionally partial pulses appear however. This is due to the random nature of the input signals, so that there will be times when coincidence occurs for intervals of time as short as a few nanoseconds. The amplitudes of these undesired spikes depend on the duration of coincidence as well as the finite rise and fall times of the detector circuitry. All the spikes will not operate a flip-flop counter directly; only those of sufficient amplitude will trip the counter. Also if a single signal from one of the coincidence detectors is fed as a common input signal to two flip-flop counters, the two paralleled counters will not count identically. This results from the fact that the two input stages will not be identical due to component tolerances and transistor differences. The more sensitive circuit will thus count smaller pulses than the less sensitive input and produce a slightly larger count at the output than the other. This action produces bias errors in the control system described in reference (a). The difficulty was largely overcome however by the introduction of a clipper and threshold amplifier ahead of the input stage of each counter. This amplifier contains three stages composed of transistors Q_{27}, Q_{28}, and Q_{29}. Its action tends to introduce a threshold level for the output signals from the coincidence detector and amplify only the spikes which exceed this to full amplitude. All full pulses of course pass through with no change. There will of course still be a narrow slice of amplitudes which still pass through with intermediate amplitudes. The number of these however is reduced by roughly the gain built into the threshold amplifier. The amplifier therefore reduces markedly the number of spurious spikes, and reduces the error between counters for identical signals to a negligible value. The effect is equivalent to what might have been obtained by the more difficult alternative of using a 10 Mc clock oscillator, and extra binary counter stages capable of accepting 10 Mc pulses to count down the extra factor of 10 in increased number of pulses.

10. A more detailed explanation of the clipper and threshold amplifier operation will now be given. The input signal, consisting mostly of negative 1 Mc pulses and scattered negative spikes, will be differentiated by the input capacitor

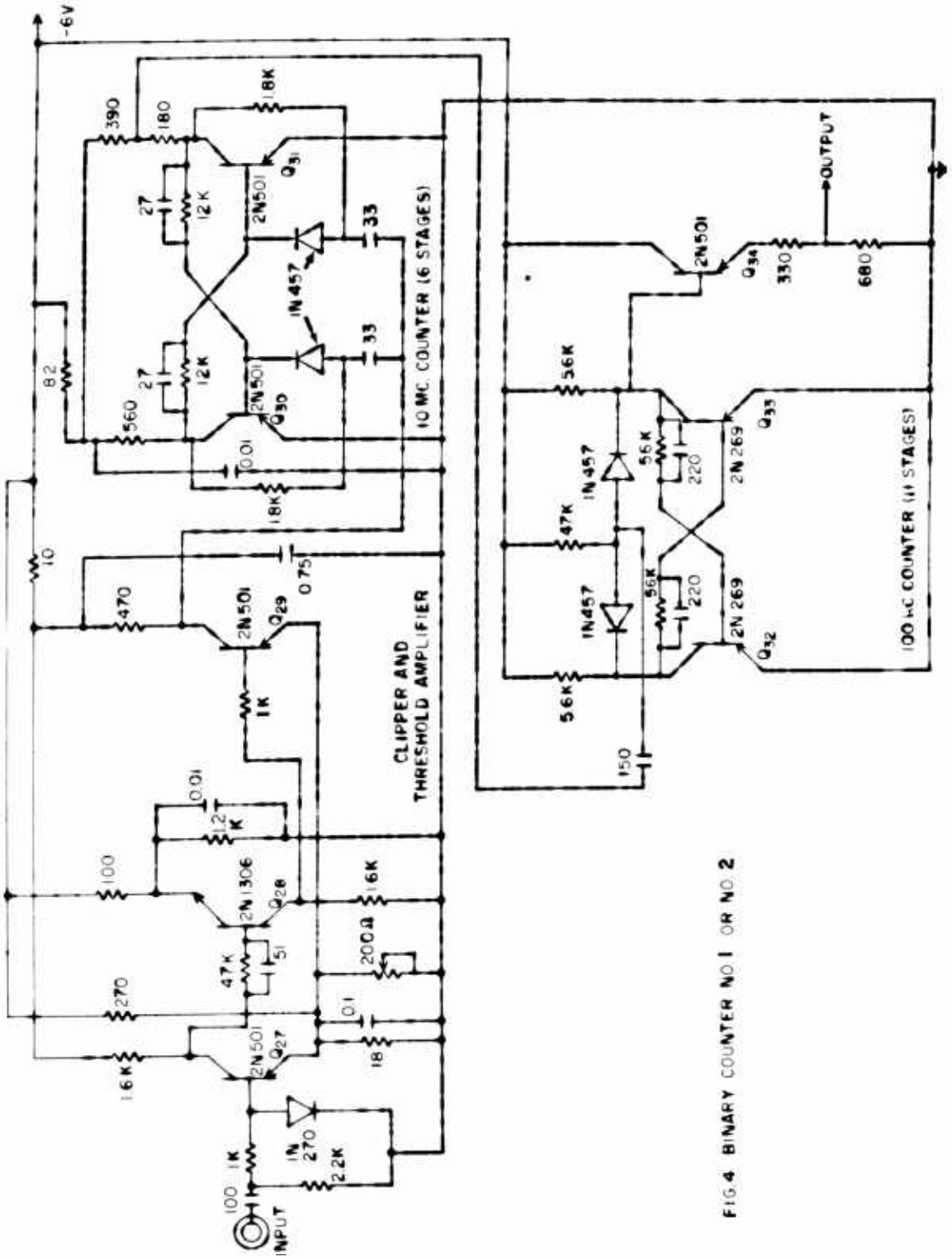

FIG 4 BINARY COUNTER NO 1 OR NO 2

and resistance. Negative and positive spikes will result from the differentiation but only the negative ones will appear at the base since the positive ones will be eliminated by the diode. The three stages consisting consecutively of a PNP transistor Q_{27}, an NPN transistor Q_{28}, and a PNP transistor Q_{29} are all normally biased beyond cut-off when no signal is present at the input. Small negative spikes which are not large enough to cause the first stage to conduct will be eliminated in the first stage and never appear in the output of the amplifier. Negative spikes which are slightly larger than required for conduction in the input stage will be amplified enough to cause saturation in the third stage, thus producing a clipping action following the threshold elimination. The net result is the production of an improved digital signal having less amplitude variation and being more suitable for driving the input counter stage. Since there are an uneven number (three) of stages of amplification, the output signal will consist of a sequence of positive-going pulses.

11. The counter itself consists of 17 stages of flip-flops in cascade. The first six stages are high frequency flip-flops capable of counting at a rate of 10 Mc. The following 11 stages are simpler, low frequency units capable of counting at 100 kc rates. Only one of each of these stages is shown in Figure 4. The configuration of the two types of flip-flops are similar, differing only in the arrangement and complexity of the steering diodes. The purpose of these is to cause the flip-flops to change from one stable state to the other only at the occurrence of positive pulses. This results in a binary count of two since the flip-flop produces a single positive output pulse for every two positive input pulses. The diodes are connected to the collectors in both styles of flip-flops in such a manner so that one diode is biased near cut-off while the other is biased several volts beyond cut-off. The polarity of the diode prevents negative pulses from reaching either base of the flip-flop, while the bias directs positive pulses to the proper base of the flip-flop to change its state. An emitter follower is employed as an output stage for the binary counter for isolation purposes. The base of this transistor is connected to the output of the proper counter stage to obtain the desired integration time.

CONSTRUCTION

12. The foregoing system of two correlators was constructed on four perforated fiber glass boards each 4-11/16" x 13-11/16" in size. The three clipper amplifiers occupied one board, the 1 Mc clock, and two polarity coincidence detectors occupied a second board; while each of the two binary counters with their

threshold amplifiers required a board. Each board was mounted to a metal framework to permit it to slide into a metal cabinet. An electrical plug fastened to one end of the perforated board provided immediate connections to the B-supply and prewired signal connections to other boards of the system when it was slid into place. The whole system occupied a volume of approximately 350 cubic inches.

CONCLUSION

13. A stable, reliable digital correlator has been built and used successfully in processing analog signals with bandwidths of 2.5 to 5.0 kc.

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SUBJECT ANALYSIS OF REPORT

DESCRIPTORS	CODES	DESCRIPTORS	CODES	DESCRIPTORS	CODES
Digital	DIGI	Polarity	POLZ	Solid-state	SOLS
Correlator (Operation)	CORLI	Coincidence	COIN	Physics	PHYS
Circuitry	CIRC	Detectors	DETT	Electronics	ELCO
Lock-in	LOCI	Multipliers	MULP		
System	SYST	Binary	BINA		
Correlator	CORL	Counters	CUNA		
Clipper	CLIP	Integrators	INTT		
Amplifiers	AMPL	Output	OUTP		
Conversion	CNVE	Single	SINL		
Analog	ANAG	Point	POIN		
Input	INPU	Correlogram	CORG		
Signals	SIGN	Acoustics	ACOU		

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1. Correlators - Circuits
2. Data processing
3. Computers, Digital
4. Computers, Analog

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